Intel ® 31154 133MHz PCI Bridge Masquerade Feature

Application Note

August 2003

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Contents

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Revision History

Date	Revision	Description
May 2003	001	This is the first release of this document.
August 2003	002	Document title change

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1.0 Introduction

The 31154 133MHz PCI Bridge (also called 31154 Bridge) is Intel's fourth generation PCI Bridge and it implements a number of new features designed to provide superior performance and functionality in both PCI and PCI-X environments.

This application note describes the implementation and usage of a unique, new feature, the Alternative ID register field, otherwise known as the "Masquerade Feature" of the 31154 133MHz PCI Bridge.

The following topics are included in this document:

- Functional Overview
- Applications
- EEPROM
- Serial ROM Interface Signals
- Serial ROM Data Format
- Serial Pre-Load Sequence

Note: This is not a stand-alone document. Please refer to the *31154 133MHz PCI Bridge Datasheet* for specific information on the 31154 features and usage.

2.0 Functional Overview

The 31154 133MHz PCI Bridge connects 2 independent PCI or PCI-X busses. The bridge has a primary interface that generally connects to the upstream Bus and a secondary interface that attaches to the downstream bus. The bridge can implement a PCI or PCI-X bus on either or both interfaces and thus can act as a translator between PCI and PCI-X bus segments.

Uses of this bridge include:

- Motherboard implementations to increase slot count.
- Option cards to allow multiple PCI or PCI-X devices to exist on the card for device loading or peer to peer traffic optimization.
- Interfacing PCI silicon into PCI-X environments without inducing the performance penalty normally associated with mixed PCI/PCI-X environments.
- Allow 5V devices to be used in 3V applications.

One of the advanced features of the 31154 Bridge is the implementation of an alternative Device ID register set that may be programmed by the system developer to change the default Vendor ID, Device ID and Revision ID reported by the device.

The "masquerade feature" allows the implementer complete control of the response by the device during system initialization and subsequent Device ID queries.

3.0 Device Masquerade Feature

The masquerade feature allows users to replace older PCI bridge devices with the 31154 Bridge with little or no impact to the device driver and operating system. It can also be used as a tool in controlling the devices installed into proprietary or mission critical applications by requiring the user defined data to be present before the device will be recognized by the system.

The basic operation of this feature is as follows:

1. When P_RST# goes inactive, the 31154 Bridge automatically executes a read from the serial EEPROM.
2. If the predetermined bit pattern is detected during the ROM load, the appropriate fields are loaded with the user provided data.
3. At the completion of the ROM load, S_RST# is de-asserted.
4. The 31154 Bridge responds to ID config cycles by reporting the user provided data.
5. This behavior persists without requiring additional accesses to the ROM or imposing additional latency until the next P_RST# event, which reloads the ROM and begins the cycle again.

4.0 EEPROM

The 31154 Bridge provides a glueless interface to a 512-Byte serial EEPROM that is used for loading 31154 Bridge configuration space register settings prior to host system discovery and initialization of the bridge. The serial ROM interface is compatible with industry standard 512-Byte Microwire* serial ROM such as Microchip Technology, Inc., 93LC66A 512x8 serial EEPROM or equivalent.

5.0 Serial ROM Interface Signals

Table 1 describes the Serial ROM Interface Signals.

Table 1. Serial ROM Interface Signals

Name	Type	Description
SR_CS	O	Serial ROM Chip Select
SR_CLK	O	Serial ROM Clock
SR_DI	O	Serial ROM Data In
SR_DO	I	Serial ROM Data Out

5.1 Serial ROM Pre-Load Operation

The serial ROM interface and optional serial ROM are used to pre-load 31154 Bridge device-specific configuration registers. This is due to assertion of P_RST# when 31154 Bridge configuration registers are reset.

Table 2 describes the two sequences that occur when emerging from secondary bus reset.

Table 2. Serial ROM Pre-Load Sequencing

P_RST#	S_RST#	SR_CS	Host Access to Bridge Configuration Space
Low	Low	Inactive	none
High	Low	Active (pre-load execution)	Retried if attempted[a]
High	High	Inactive (pre-load complete)	Accessible by host

a. If the31154 Bridge is configured for Compact PCI Hot Swap mode (HS_SM = 1), host access will be ignored resulting in a Master Abort on the primary interface.

The 31154 Bridge automatically executes a serial read from the ROM once P_RST# has gone inactive. S_RST# is de-asserted once the Serial ROM preload operation has completed. All 31154 Bridge initialization data is loaded with a single read operation by keeping the chip select asserted and toggling the clock. All throughout the Serial ROM pre-load process 31154 Bridge retries any configuration accesses until the pre-load sequence has completed.

The pre-load sequence takes approximately 570 ∝sec. if P_PCLK is operating at 33 MHz (approximately 550 cycles * 1.08 ∝sec./cycle).

If the serial ROM is present, but a register pre-load is not desired, bits [7:6] of the first byte (the first two bits read) should read as any value except the pre-load enable value (i.e.,10b).

If the 31154 Bridge does not detect the pre-load enable two bit sequence, it stops the pre-load operation. In this case, all serial ROM pre-loadable configuration registers remain at their reset default values.

Note: If the optional Serial ROM is not deployed, the VPD Capability List registers are made invisible to PCI bus scans.

6.0 Serial ROM Data Format

Table 3 details the layout of the Serial ROM.

Note: Only a subset of the 31154 Bridge internal registers are Serial ROM pre-loadable. Reserved or unused bits must be written to 0b when formatting the Serial ROM contents.

The clock input to the serial ROM is approximately 500 KHz and is established by dividing down the primary bus clock input (P_PCLK). The duty cycle is approximately 50%.

Table 3. Serial Pre-Load Sequence (Sheet 1 of 2)

Byte offset	Description
00h	[7:6] 10b to enable serial pre-load [5:0] 000001b (load Vendor ID/Device ID/Revision ID) [5:0] 000000b (Reserved)
01h	Arbiter Control / Status[7:0]
02h	Arbiter Control / Status[15:8]
03h	31154 Control Register 0
04h	31154 Control Register 1[7:0]
05h	31154 Control Register 1[15:8]
06h	31154 Control Register 2[7:0]
07h	31154 Control Register 2[15:8]
08h	Multi-Transaction Timer Register[7:0]
09h	Multi-Transaction Timer Register[15:8]
0Ah	Pre-Fetch Policy Register[7:0]
0Bh	Pre-Fetch Policy Register[15:8]
0Ch	P_SERR# Assertion Control Register[7:0]
0Dh	P_SERR# Assertion Control Register[15:8]
0Eh	Secondary IDSEL Select Register[7:0]
0Fh	Secondary IDSEL Select Register[15:8]
10h	Secondary IDSEL Fnct 0 Enable Register[7:0]
11h	Secondary IDSEL Fnct 0 Enable Register[15:8]
12h	GPIO Pin Configuration Register
13h	GPIO Write One to Toggle Register
14h	Opaque Memory Base and Limit Register[7:0]
15h	Opaque Memory Base and Limit Register[15:8]
16h	Opaque Memory Base and Limit Register[23:16]
17h	Opaque Memory Base and Limit Register[31:24]
18h	Opaque Memory Base Upper 32 Bits[7:0]
19h	Opaque Memory Base Upper 32 Bits[15:8]
1Ah	Opaque Memory Base Upper 32 Bits[23:16]
1Bh	Opaque Memory Base Upper 32 Bits[31:24]
1Ch	Opaque Memory Limit Upper 32 Bits[7:0]
1Dh	Opaque Memory Limit Upper 32 Bits[15:8]
1Eh	Opaque Memory Limit Upper 32 Bits[23:16]
1Fh	Opaque Memory Limit Upper 32 Bits[31:24]
20h	Slot Number Register
21h	Chassis Number Register
22h	Power Management Next Item Pointer: Must be pre-loaded with a value of E4h to expose VPD register block to software.
23h	Power Management Capabilities Register[15:8] This register may be pre-loaded with high order bits [15:11] set to 11111b indicating that the bridge supports PME# generation from any PM DState. This feature may be used to workaround a Windows 98 bridge power management errata.

Table 3. Serial Pre-Load Sequence (Sheet 2 of 2)

Byte offset	Description
24h	ID [7:0] The Device ID and Vendor ID are only preloaded if SROM offset 00h = 1000_0001. Otherwise, offsets 24h-28h are ignored.
25h	ID [15:8].
26h	ID [23:16].
27h	ID [31:24].
28	RID The Revision ID is only preloaded if SROM offset 00h = 1000_0001. Otherwise, offsets 24h-28h are ignored.
29h - 7Fh	Reserved.
80h - 0FFh	Vital Product Data (Read Only region).
100h - 1FFh	Vital Product Data (Read / Write region).

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